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Bing Lu, Jiang Hu, Process variation aware clock tree routing to avoid a suboptimal design and excessive violations due to single critical

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CAO et al.: WIRE SIZING AND SPACING FOR LITHOGRAPHIC PRINTABILITY AND TIMING OPTIMIZATION 1333 Fig. 3. OPC results in fractures in mask layout [6].

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Authors: Tetsuya Iizuka: Department of Electronic Engineering, University of Tokyo, Tokyo, Japan:
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two-level logic circuits are of limited importance in a very-large-scale integration (VLSI) design; optimization and design automation: synthesis,

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